IFW

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Gerchih CHOU et al

Art Unit: 2661

Application No: 10/685,560

Examiner:

Filed: October 14, 2003

For: ADAPTIVE EQUALIZATION SYSTEM FOR A SIGNAL RECEIVER

PRELIMINARY AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

Please make the following amendments to this application prior to examination thereof.

DESCRIPTION AMENDMENTS

Rewrite paragraph [0020] to read as follows:

FIG. 3 illustrates the ~~CRD~~ CDR unit of FIG. 2 in more detailed block diagram form.

Rewrite paragraph [0033] to read as follows:

A clock and data recovery (CDR) unit 50 therefore processes signal X to generate a 50% duty cycle sampling clock signal CLK having plurality of successive cycles of substantially uniform duration wherein each leading edge of the sampling clock signal occurs at a start of each sampling clock signal cycle and each trailing edge of the sampling clock occurs substantially midway through each sampling clock signal cycle. ~~CRD unit 50~~ CDR unit 50 adjusts the phase and frequency of sampling clock signal CLK so that trailing edges of the sampling clock signal occur when compensated signal X is transitioning between states, thereby ensuring that by sampling compensated signal X on each leading edge of the sampling clock signal, ~~CRD unit 50~~ CDR unit 50 can produce an output first data signal Z having a succession of states representing the succession of symbols conveyed by transmitted signal VX. In the examples provided herein, each rising edge of sampling clock signal CLK is treated as a "leading" edge and each falling edge is treated as a "trailing" edge of the sampling clock signal. However, those of skill in the art will appreciate that clock signal polarity is a matter of design choice and that in alternative embodiments of the invention, falling edges may be treated as leading edges and rising edges may be treated as trailing edges.

Rewrite paragraph [0041] to read as follows:

FIG. 14 illustrates feedback equalizer unit 94 of FIG. 13 in more detail. Producing the offset signal F signal input to summing amplifier 88 as functions of the G1, G2 and Z signals, feedback equalizer unit 94 suitably includes a latch 95, a pair of amplifiers 96 and 97 having gains controlled by filter control signals G1 and G2, and a summing amplifier 98. First data signal Z drives amplifier 97. The output of latch 95, representing the state of first data signal Z on each trailing edge of the CLK signal, provides an amplifier 96 input. Summing amplifier 98 generates offset signal F as a sum of outputs of amplifiers 96 and 97. Adaptation control circuit 92 of FIG. 13 suitably implements, for example, the following adaptation algorithm:

$G1_{n+1} = G1_n + \Delta_+$ when $S_{n-1} = Z_{n-2}$, else $G1_n + 1 = G1_n - \Delta_-$

~~$G2_{n+2} = G2_n + \Delta_+$ when $S_{n-1} = Z_{n-3}$, else $G2_n + 2 = G2_n - \Delta_-$~~

$G2_{n+2} = G2_n + \Delta_+$ when $S_{n-1} = Z_{n-3}$, else $G2_{n+1} + 2 = G2_n - \Delta_-$

where

$G1_n$ is a magnitude of the first filter control signal during an n^{th} sampling clock signal cycle,

$G1_{n+1}$ is a magnitude of the first filter control signal during an $(n+1)^{th}$ sampling clock signal cycle,

$G2_n$ is a magnitude of the second filter control signal during the n^{th} sampling clock signal cycle,

$G2_{n+1}$ is a magnitude of the second filter control signal during the $(n+1)^{th}$ sampling clock signal cycle,

Z_{n-2} is a state of the first data signal following an $(n-2)^{th}$ trailing edge of the sampling clock signal

Z_{n-3} is a state of the first data signal following an $(n-3)^{th}$ trailing edge of the sampling clock signal,

S_{n-1} is a state of the second data signal following an $(n-1)^{th}$ trailing edge of the sampling clock signal, and

Δ_+, and Δ_- are constants.

Adaptation control circuit 92 increases G1 when S_{n-1} is of the same sign as Z_{n-2} because this indicates that signal X is under-compensated. Otherwise, adaptation control circuit 92 considers signal X to be over-compensated and decreases G1. Similarly, adaptation control circuit 92 increases G2 when S_{n-1} is of the same sign as Z_{n-3} because this indicates that signal X is under-compensated. Otherwise, adaptation control circuit 92 considers signal X to be over-compensated and decreases G2.